English translation of the selected parts of Japanese Unexamined Patent Application Publication No. 2000-322375.

[0029]

FIG. 6 is a drawing for explaining the content of the operation of each block in the FIFO control shown in FIG. 2. The FIFO control register 205 is a register for determining an operation mode of FIFO. The transfer byte number register 206 is a register for setting the burst length executed per a single DMA transfer, wherein, based on the set value, it controls the transfer byte counter A207 and the transfer byte counter B208 so as to change the burst length in a programmable manner. The transfer byte counter A207 is a counter for counting the signal ACK-A output from the DMAC 104; and the transfer type counter B208 is a counter for counting the signal ACK-B output from the FIFO. Based on respective count values, the states of the FIFO-A and FIFO-B are judged, thus controlling the output timing with respect to the selector control signal, signal REQ-A, and signal ACK-B.

[0030]

In addition, the initial values of the transfer byte counter A207 and the transfer byte counter B208 differ in response to data transfer directions, wherein when the FIFO receives data, the number of reception times is set up. When the FIFO receives data, the initial value is zero; but when the FIFO loads transmission data from the other FIFO, the number of transmission times is set up. The number of reception times and the number of transmission times are set up based on the value of the transfer byte number register 206.

[FIG. 2]

105 32-BIT DATA BUS
109 16-BIT DATA BUS
201 FIFO
202 FIFO CONTROL
205 FIFO CONTROL REGISTER
206 TRANSFER BYTE NUMBER REGISTER
207 TRANSFER BYTE COUNTER A
208 TRANSFER BYTE COUNTER B
209 BYPASS SWITCH

[FIG. 6]

Register Name	R/W	Bit	Description
205 FIFO CONTROL REGISTER	R/W	0	FIFO mode switch bit Switch over between configuration mode and operation mode 0: configuration mode 1: operation mode
		1	Dir Switch over data transfer direction 1: A → B 0: B → A
		2	BypsOe Directly connect data bus without use of FIFO 1: bypass 0: non-bypass
		3	reserved
		4:5	FIFO-A bit number conversion FIFO-A bit number change 0: 8 bits 1: 16 bits 2: 32 bits 3: reserved
		6:7	FIFO-B bit number conversion FIFO-B bit number change 0: 8 bits 1: 16 bits 2: 32 bits 3: reserved
206 TRANSFER BYTE NUMBER REGISTER	R/W	0:7	Set up transfer burst length per single DMA Based on the set value, transfer byte counters A, B are controlled, thus enabling transfer of 1-256 byte length
207 TRANSFER BYTE COUNTER A	R	0:7	Count transfer byte number (ACK-A number) of FIFO-A, thus controlling REQ-A signal Initial value is set in response to the following data transfer direction A→B: data reception times B→A: 0 (Upon loading of transmission data from FIFO-B, transmission times is set up)

208 TRANSFER BYTE COUNTER B	R	0:7	Count transfer byte number (ACK-B number) of FIFO-B, thus controlling ACK-B signal Initial value is set in response to the following data transmission direction B→A: data reception times A→B: 0 (Upon loading of transmission data from FIFO-A, transmission times is set up)